REMARKS

In response to the Non-Final Office Action dated February 28, 2006, Applicants respectfully request reconsideration based on the above claim amendments and the following remarks. Applicants respectfully submits that the claims as presented are in condition for allowance.

Claims 1-24, 26, 27, 30 and 31 are pending in the present Application. Claims 8 and 19 are amended leaving Claims 1-24, 26, 27, 30 and 31 for consideration upon entry of the present amendment and following remarks.

Support for the amendments are at least found in the specification, the figures, and the claims as originally filed.

No new matter has been introduced by these amendments. Reconsideration and allowance of the claims are respectfully requested in view of the above amendments and the following remarks.

Claim Rejections – 35 U.S.C. §112

The Examiner has rejected Claims 8 and 19 under 35 U.S.C. 112, second paragraph as failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner states that the term "wherein the semiconductor layer corresponds to the first connecting lines" in Claims 8 and 19 is a relative term which renders the claims indefinite, is not defined by the claim and the specification does not provide a standard for ascertaining the requisite degree. The Examiner alleges that it is not clearly defined as to how the semiconductor layer corresponds to the first connecting lines. For purposes of examination, Claims 8 and 19 are interpreted as meaning wherein the semiconductor layer is formed in the peripheral area underlying the second connecting lines as shown in Fig. 4 of the Drawings acting as another insulating layer between the first and second connecting lines.

In response, Applicants amend Claims 8 and 19 to include "the semiconductor layer is formed underlying the first connecting lines." Applicants respectfully submit that Claims 8 and 19 satisfy the provisions of 35 USC §112, second paragraph.

Reconsideration and withdrawal of the relevant rejections of Claims 8 and 19 are respectfully requested.

Claim Rejections Under 35 U.S.C. §103

Regarding Claims 1, 2, 4-7, 9, 10, 12, 13, 15-18, 20 and 21

Claims 1, 2, 4-7, 9, 10, 12, 13, 15-18, 20 and 21 under 35 U.S.C. §103(a) as being unpatentable over Takahashi et al., U.S. Patent Publication 2003/0063080 (hereinafter Takahashi A") in view of Takahashi et al., U.S. Patent Publication 2003-0112382 (hereinafter "Takahashi B"). Applicants respectfully traverse.

For an obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art; and that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In Re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970).

Firstly, independent Claims 1, 10, 12 and 21 recite, *inter alia*,

"a first connecting part, formed in the second peripheral region to be coupled to the first ends of the scan lines, the first connecting part including a plurality of groups, each of the groups disposed in layers different from each other, the scan driving signal being applied to the first connecting part."

In the Office Action, the Examiner has stated that Takahashi A discloses all elements of the claimed subject matter, excluding *that each groups of the first connecting part is disposed in layers different from each other* of Claims 1, 10, 12 and 21, which the Examiner has stated is disclosed by Takahashi B in Figure 8 and at paragraphs 0175-0176. Applicant respectfully disagrees.

Takahashi B discloses the gate (scanning) lines GL and drain (data) lines DL form rectangular areas serving as pixel regions and an aggregate of these pixel regions constitute a display region AR. (Paragraph [0124] and FIG. 1.) At each end of the GL and DL is formed the terminal GTM and DTM, respectively, connected to bumps of semiconductor integrated circuits, GDRC and DDRC, respectively. (Paragraphs [0129]

and [0130] and FIG. 1.) Bumps of the GDRC and DDRC on the input side (separate from those connected on the output side proximate the ends of the GL and DL) are connected to terminals GTM2 and DTM2, respectively, further connected to corresponding terminals GTM3 and DTM3, respectively, via wiring layers GIL and DIL, respectively. (Paragraph [0132] and FIG. 1.) That is, Takahashi B distinguishes the signal lines (GIL,DIL) on the input side of the semiconductor integrated circuits (GDRC,DDRC) from the separate gate and data lines (GL,DL).

Paragraphs [0173] to [0178] describe "Structure of Signal Lines on **Input Side** of Semiconductor Integrated Circuit" relative to FIG. 8. Here, spacing of the **input lines** GIL,DIL may be disposed in different layers (PSV,GI). The input lines GIL,DIL as discussed above, are separate from the gate and data lines (GL,DL) and are outside of the semiconductor integrated circuits GDRC,DDRC. That is, the input lines GIL,DIL, being relied upon as teaching the "first connecting part disposed in different layers" of the claimed invention, are in no way coupled to the first ends of the scan lines.

Therefore, Takahashi A and Takahashi B do not disclose "a first connecting part, formed in the second peripheral region to be *coupled to the first ends of the scan lines*, the first connecting part including a plurality of groups, each of the groups *disposed in layers different from each other*, the scan driving signal being applied to the first connecting part" of Claims 1, 10, 12 and 21.

Secondly, Claims 1, 10, 12 and 21 recite, *inter alia*,

"the scan driving circuit providing the scan lines with a scan driving signal and the scan driving signal being applied to the first connecting part."

Since the input lines GIL,DIL, being considered the first connecting part of the claimed invention, are on the input side (or before) the semiconductor integrated circuits GDRC,DDRC, "the scan driving signal from the scan driver circuit" of Claims 1, 10, 12 and 21, necessarily cannot be applied to the input lines GIL,DIL. That is, the input lines GIL,DIL, further do not disclose "the first connecting part" of the claimed invention.

Therefore, Takahashi A and Takahashi B do not disclose "*the scan driving circuit providing the scan lines with a scan driving signal* and a first connecting part formed in

the second peripheral region to be coupled to the first ends of the scan lines, the first connecting part including a plurality of groups, each of the groups disposed in layers different from each other, *the scan driving signal being applied to the first connecting part*" of Claims 1, 10, 12 and 21.

Finally, regarding Claims 7 and 18, the Examiner states that Takahashi B discloses in Figures 11A-11D that the first insulating layer (elements GI and AS combined) includes the second insulating layer (element GI) and the semiconductor layer (element AS). Applicants respectfully disagree.

Claims 7 and 18 variously depend from Claims 1 and 12, respectively, and inherit all of the limitations of Claims 1 and 23 and the intervening claims. The first connecting part formed in the peripheral region (Claims 1 and 12) comprises first and second connecting lines (Claims 2 and 13) with the first insulating layer interposed between the first and second connecting lines (Claims 4 and 15). That is, the first insulating layer is disposed in the peripheral region.

Figure 11A of Takahashi B discloses the semiconductor layer AS and the insulation layer GI formed in the TFT area of the display region. Therefore, Takahashi A and Takahashi B do not disclose the first insulation layer includes the second insulation layer and the semiconductor layer of Claims 7 and 18.

As discussed above, Takahashi A and Takahashi B *do not teach or suggest all of the limitations* of at least Claims 1, 7, 10, 12, 18 and 21. Thus, *prima facie* obviousness does not exist regarding Claims 1, 7, 10, 12, 18 and 21with respect to Takahashi A and Takahashi B.

Applicants further submit that there exists *no motivation to modify or combine* Takahashi A and Takahashi B to teach the claimed invention. As detailed above, Takahashi B distinguishes the signal lines (GIL,DIL) on the input side of the semiconductor integrated circuits (GDRC,DDRC) from the separate gate and data lines (GL,DL). Applicants find no disclosure or suggestion in Takahashi B to use the structure of the *input* lines clearly outside of the semiconductor integrated circuits GDRC,DDRC

to the connecting part of Takahashi A, especially since the scan driving signal from the scan driver circuit, necessarily is not applied to the input lines GIL,DIL.

Since Takahashi A and Takahashi B fail to teach or suggest all of the limitations of Claims 1, 7, 10, 12, 18 and 21and that there lacks evidence to show that knowledge generally available to one of ordinary skill in art would lead that individual to combine the relevant teachings of the references to disclose the claimed invention, clearly, one of ordinary skill at the time of Applicant's invention would not have a *motivation to modify or combine the references*, nor a reasonable likelihood of success in forming the claimed invention by the Examiner's modifying or combining the references. Thus, here again, *prima facie* obviousness is unfounded. *Id.*

Thus, the requirements of *prime facie* obviousness are not met by the Examiner's 35 U.S.C. 103(a) rejection of Claims 1, 7, 10, 12, 18 and 21 with respect to Takahashi A and Takahashi B. Applicants respectfully submit that Claims 1, 7, 10, 12, 18 and 21are not further rejected or objected and are therefore allowable to Applicants. Claims 2, 4-6, 9, 13, 15-17 and 20 variously depends from Claims 1 and 12 and are correspondingly allowable. Reconsideration, withdrawal of the relevant rejections and allowance of Claims 1, 2, 4-7, 9, 10, 12, 13, 15-18, 20 and 21 are respectfully requested.

Regarding Claims 3, 8, 14, 19, 23, 24, 26, 27, 30 and 31

Claims 3, 8, 14, 19, 23, 24, 26, 27, 30 and 31 are rejected under 35 U.S.C. §103(a) as being unpatentable over Takahashi A and Takahashi B in view of Ishige et al., U.S. Patent Publication 2004/0012744 (hereinafter "Ishige"). Applicants respectfully traverse.

Applicants submit herewith a certified translation of the priority document, Korean Patent Application No. 2002-56070, which was filed on September 16, 2002. Because this priority document was filed before the publishing date and filing date, January 22, 2004 and July 15, 2003 respectively, of Ishige, Applicants have properly antedated Ishige. Accordingly, Applicants respectfully request that all of the Examiner's rejections in which Ishige is used as a reference be withdrawn.

Notwithstanding that Ishige has been properly antedated, Applicants respectfully submit that Ishige also does not teach all of the limitation of the claimed invention and does not remedy the deficiencies of Takahashi A and Takahashi B.

Claims 3, 8, 14 and 19 variously depend from Claims 1 and 12 and inherit all of the limitations of Claims 1 and 12. As discussed above, Claims 1 and 12 are allowable over Takahashi A and Takahashi B. Claims 24, 26 and 27 depend from Claim 23 and inherit all of the limitations of Claim 23.

Independent Claims 23, 30 and 31 recite, *inter alia*, forming a substrate wherein each of the groups of the first connecting part is disposed in layers different from each other and that the first connecting lines partly overlaps with at least one of the secondary connecting lines. For all the reasons discussed above relative to Claims 1 and 12, Takahashi A and Takahashi B do not disclose "the scan driving circuit providing the scan lines with a scan driving signal and a first connecting part formed in the second peripheral region to be coupled to the first ends of the scan lines, the first connecting part including a plurality of groups, each of the groups disposed in layers different from each other, the scan driving signal being applied to the first connecting part."

Ishige is relied upon as teaching the first connecting lines partly overlap with at least one of the second connecting lines. Applicants find no disclosure in Ishige as teaching forming a substrate or a substrate wherein in each of the groups of the first connecting part is disposed in layers different from each other and that the first connecting lines partly overlaps with at least one of the secondary connecting lines of the claimed invention. Therefore, Ishige does not remedy the deficiencies of Takahashi A and Takahashi B with respect to independent Claims 1, 12, 23, 30 and 31.

Takahashi A, Takahashi B and Ishige fail to each all of the limitations of Claims 3 and 8 (depending from Claim 1), Claims 14 and 19 (depending from Claim 12) and Claims 23, 24, 26, 27, 30 and 31. Thus, the requirements of *prime facie* obviousness are not met by the Examiner's 35 U.S.C. 103(a) rejection of Claims 3, 8, 14, 19, 23, 24, 26, 27, 30 and 31. Applicants respectfully submit that Claims 3, 8, 14, 19, 23, 24, 26, 27, 30 and 31 are not further rejected or objected and are therefore allowable to Applicants.

Reconsideration, withdrawal of the relevant rejections and allowance of Claims 3, 8, 14, 19, 23, 24, 26, 27, 30 and 31 are respectfully requested.

Regarding Claims 3, 8, 14, 19, 23, 24, 26, 27, 30 and 31

Claims 11 and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Takahashi A and Takahashi B in view of Tsuyuki et al., U.S. Patent No. 6,853,361 (hereinafter "Tsuyuki"). Applicants respectfully traverse.

Claims 11 and 22 variously depend from Claims 1 and 22, respectively, and inherit all of the limitations of their parent claims. As discussed above, Claims 1 and 22 are allowable over Takahashi A and Takahashi B. Tsuyuki is relied upon as disclosing the first connecting part is electrically coupled to odd numbered scan lines and the second connecting part is electrically coupled to even numbered scan lines. Applicants find no disclosure in Tsuyuki as teaching *the scan driving circuit providing the scan lines with a scan driving signal* and a first connecting part formed in the second peripheral region to be coupled to the first ends of the scan lines, the first connecting part including a plurality of groups, each of the groups disposed in layers different from each other, *the scan driving signal being applied to the first connecting part* of the claimed invention. Therefore, Tsuyuki does not remedy the deficiencies of Takahashi A and Takahashi B with respect to Claims 11 and 22.

Takahashi A, Takahashi B and Tsuyuki fail to each all of the limitations of Claims 11 and 22. Thus, the requirements of *prime facie* obviousness are not met by the Examiner's 35 U.S.C. 103(a) rejection of Claims 11 and 22. Applicants respectfully submit that Claims 11 and 22 are not further rejected or objected and are therefore allowable to Applicants. Reconsideration, withdrawal of the relevant rejections and allowance of Claims 11 and 22 are respectfully requested.

Conclusion

In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance issued.

The Examiner is invited to contact Applicants' attorney at the below listed phone number regarding this response or otherwise concerning the present application.

Applicants hereby petition for any necessary extension of time required under 37 C.F.R. 1.136(a) or 1.136(b) which may be required for entry and consideration of the present Reply.

If there are any charges due with respect to this Amendment or otherwise, please charge them to Deposit Account No. 06-1130 maintained by Applicants' attorneys.

Respectfully submitted,

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